Harshvardhan Rathod

+91 77092 85391 hmr280606@gmail.com LinkedIn: harshvardhan-rathod GitHub: HAPPIOcrz007

Codeforces: Harshvardhan_Rathod (980+) **CodeChef:** happiocrz_007 (1300+, 2⋆)

Education

Dr. Vishwanath Karad MIT World Peace University — Kothrud, Pune
B.Tech, Electronics & Computer Engineering — SGPA: 8.88 (Sem I) — *Aug. 2025 – Present*

Aarham College, Camp — Pune
HSC (12th), Science — 73.22% — *2024 – 2025*

The Bishop's School, Camp — Pune
ICSE (10th) — 96.8% — *2022 – 2023*

Experience

Pravii Technologies and Industry Solutions — Pune, India
Software Developer Intern — *Feb. 2026 – Present*

- Recruited directly (without application) to develop a Physics and Optics Analysis Tool that simulates optical systems and performs matrix-based computations.
- Architecting matrix optimisation pipelines with OS-level and system-level tuning to minimise computation overhead on constrained hardware.
- Applying low-latency programming techniques and memory management strategies relevant to real-time scientific simulation workloads.

CODEC — Competitive Programming Club, MITWPU — Pune, India
Head of Management — *Nov. 2025 – Present*

- Managed budgeting, accounting, and financial approvals for a 100-member, 4-year-old department-level club focused on ICPC and CP/DSA growth.
- Coordinated tripartite communication between faculty mentors, AlgoZenith (speakers, problem sets), and Prism Labs (volunteer management) for large-scale events.
- Assisted in hosting and management of *Trifecta*, a 250+ participant competitive programming event organised by the club.

Projects

Stock Market Edge Simulator | *C++, Multithreading, Low-Latency Systems* | 2026

- Building a high-performance stock exchange simulator featuring a multithreaded matching engine with lock-free order processing.
- Implementing a memory-managed order book following a small-pipe architecture to minimise cache misses and memory allocation overhead.
- Applying OS-level optimisations (CPU affinity, NUMA awareness, kernel bypass concepts) to achieve sub-microsecond order matching latency targets.

4×4 Register Read/Write Controller | *74-Series TTL ICs, PCB Design* | 2025 – 2026

- Designed and fabricated a custom PCB implementing a 4×4 memory register array using 74-series TTL ICs with synchronous read/write and asynchronous clear (PIPO architecture).
- Engineered an intuitive physical interface prioritising hands-on learnability; presented working prototype at college hardware hackathon (finalist).
- Project adopted by the college as a recommended learning kit for junior-year students in digital electronics.

Achievements

76th / 2000+ in *Code Uncode* — inter-collegiate CP contest by COEP Pune, SPIT & DJSCE Mumbai; selected for finals.

76th / 759 teams in *Impulse* — CP contest by Scaler School of Technology, Bengaluru; selected for finals.

980+ rating on Codeforces; **1300+ rating (2⋆)** on CodeChef; active competitive programmer across CF, LeetCode, CSES, and AlgoZenith.

Technical Skills

Languages: C++, C, Python, Java, SQL, HTML/CSS, JavaScript
Systems & Tools: Linux, Bash, Git, VS Code, Android Studio, Jenkins
Domains: Low-Latency Programming, Memory Management, OS Optimisation, Digital Electronics, PCB Design
Platforms: Codeforces, CodeChef, LeetCode, CSES, AlgoZenith